What is claimed is:

1. A non-volatile semiconductor storage apparatus comprising:

a memory cell array which has unit cells arranged in a matrix shape, said unit cell including:

a memory cell field effect transistor having a floating gate and a control gate; and

a select field effect transistor having a drain connected to a source of said memory cell field effect transistor, said floating gate and control gate extending to a position above a gate of said select field effect transistor.

2. A non-volatile semiconductor storage apparatus having a memory cell array having unit cells, said unit cell including a memory cell field effect transistor and a select field effect transistor, said memory cell field effect transistor having a floating gate and a control gate, and said select field effect transistor having a drain connected to a source of said memory cell field effect transistor, said storage apparatus comprising:

a first semiconductor layer composing a portion of said floating gate and a gate of said select field effect transistor;

a second semiconductor layer formed on said first semiconductor layer in said memory cell field effect transistor, composing another portion of said floating gate and extending to a position above said gate of said select field effect transistor;

a first insulation layer which insulates said first semiconductor layer from said second semiconductor layer in said select field effect transistor;

a second insulation layer formed on said second semiconductor layer; and

a third semiconductor layer formed on said second insulation layer and composing said control gate.

3. The non-semiconductor storage apparatus according to claim 1 comprising:

a source line commonly connecting sources of said select field effect transistors arranged in a first direction; and

a semiconductor layer connecting said source and said source line for said each select field effect transistor.

4. The non-semiconductor storage apparatus according to claim 2, further comprising:

a source line commonly connecting sources of said select field effect transistors arranged in a first direction; and

a semiconductor layer connecting said source and said source line for said each select field effect transistor.

5. The non-volatile semiconductor storage apparatus according to claim 1, further comprising a drain diffusion layer shared between adjacent memory cell field effect transistors in a second direction in said unit cells.

6. The non-volatile semiconductor storage apparatus according to claim 2, further comprising a drain diffusion layer shared between adjacent memory cell field effect

~~transistors in a second direction in said unit cells.~~

7. The non-volatile semiconductor storage apparatus according to claim 3, further comprising a drain diffusion layer shared between adjacent memory cell field effect transistors in a second direction in said unit cells.

8. The non-volatile semiconductor storage apparatus according to claim 4, further comprising a drain diffusion layer shared between adjacent memory cell field effect transistors in a second direction in said unit cells.

9. A manufacturing method of a non-volatile semiconductor storage apparatus having a memory cell array having unit cells, said unit cell including a memory cell field effect transistor and a select field effect transistor, said memory cell field effect transistor having a floating gate and a control gate, and said select field effect transistor having a drain connected to a source of said memory cell field effect transistor, said method comprising the steps of:

forming a portion of said floating gate of a same semiconductor layer as a gate of said select field effect transistor;

forming another portion of said floating gate to extend to a portion above said gate of said select field effect transistor; and

forming said control gate so as to be superimposed on said floating gate in a planar view.

10. The manufacturing method of a non-volatile semiconductor storage apparatus according to claim 9,

wherein in forming another portion of said floating gate, a first semiconductor layer connected to a source of said select field effect transistor is formed of a same semiconductor layer as said another portion, and in forming said control gate, a second semiconductor layer is formed of a same semiconductor layer as said control gate on said first semiconductor layer.

11. The manufacturing method of a non-volatile semiconductor storage apparatus according to claim 10, wherein in forming said first semiconductor layer, impurities is introduced into said first semiconductor layer to reduce a resistance of said first semiconductor layer.

12. The manufacturing method of a non-volatile semiconductor storage apparatus according to claim 9, wherein in forming a portion of said floating gate, said semiconductor layer is patterned at the same time as said gate of said select field effect transistor.

13. The manufacturing method of a non-volatile semiconductor storage apparatus according to claim 10, wherein in forming a portion of said floating gate, said semiconductor layer is patterned at the same time as said gate of said select field effect transistor.

14. The manufacturing method of a non-volatile semiconductor storage apparatus according to claim 11, wherein in forming a portion of said floating gate, said semiconductor layer is patterned at the same time as said gate of said select field effect transistor.

15. The manufacturing method of a non-volatile

semiconductor storage apparatus according to claim 9, wherein forming a portion of said floating gate is performed after forming said gate of said select field effect transistor.

16. The manufacturing method of a non-volatile semiconductor storage apparatus according to claim 10, wherein forming a portion of said floating gate is performed after forming said gate of said select field effect transistor.

17. The manufacturing method of a non-volatile semiconductor storage apparatus according to claim 11, wherein forming a portion of said floating gate is performed after forming said gate of said select field effect transistor.

18. The manufacturing method of a non-volatile semiconductor storage apparatus according to claim 9, further comprising the steps of:

forming a source line commonly connecting sources of said select field effect transistors arranged in a first direction; and

forming a bit line commonly connecting drains of said memory cell field effect transistors in a second direction, said second direction being orthogonal to said first direction.